REMARKS

As a preliminary matter, Applicants thank the Examiner for the courtesy extended to their attorney, B. Joe Kim, in a telephone interview on October 4, 2005. In the interview, Fig. 5C of the application was compared with the structures shown in the cited references. The Examiner acknowledged that there appears to be some differences between Fig. 5C and the structures shown in the cited references. The Examiner advised that he would give further consideration to Applicants' positions if submitted in a formal response, and at least remove the finality of the Office Action, if warranted. The subject Amendment reflects Applicants' positions presented in the telephone interview.

The Examiners allowance of claims 7 and 8 is acknowledged and appreciated.

Claims 5 and 6 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Yamazaki et al. (U.S. 6,603,453) in view of Yamazaki et al. (US 2001/0052950 A1) and Kawasaki et al. Applicants respectfully traverse this rejection, because the cited references, even if combined, still would not disclose or suggest the first gate electrode being formed on the second and first gate insulation films (the second gate insulation film being formed on the first gate insulation film), and the second gate electrode being formed between the first gate insulation film and the second gate insulation film (see Fig. 5C).

The present invention includes a first thin film transistor (TFT) and a second thin film transistor (TFT). The first TFT includes a first gate electrode formed on a second gate insulation film, which is formed on the first gate insulation film, which in turn is formed on a semiconductor layer on a substrate. The second TFT includes a second gate electrode

which is formed between the first gate insulation film and the second gate insulation film, instead of being formed on the second gate insulation film, as with the first gate electrode of the first TFT. The first and second gate insulation films are the same in both the first and second TFTs.

As recognized by the Examiner, the Yamazaki et al. '498 reference does not disclose any gate insulation layer (first or second) being formed over a semiconductor layer.

The Yamazaki et al. '950 reference is cited merely for disclosing a gate insulation layer being formed over a semiconductor layer and having a lightly doped region. However, as with the Yamazaki et al. '453 reference, Yamazaki et al. '950 also does not disclose or suggest a first electrode being formed on second and first gate insulation films, and a second gate electrode being formed between the second and first gate insulation films.

Claim 1 of the Kawasaki et al. reference is cited as disclosing "the require gate electrode between gate insulating layers." Claim 1 of Kawasaki et al. recites "a first gate electrode formed between the first gate insulating film and the substrate" (see col. 23, lines 54-55), and "a second gate electrode formed between the second gate insulating film and the substrate" (see col. 23, line 63-63). In other words, the first and second gate electrodes are each formed between an insulating film (either first or second) and the substrate. In contrast, the first gate electrode of the present invention is formed on both the first and second gate insulation films and the second gate electrode is formed between the first and second insulation films, and not between an insulating film and the substrate.

As described above, none of the cited references disclose or suggest at least the first gate electrode being formed on the second and first gate insulation films (where the second gate insulating film is formed on the first gate insulation film), and a second gate electrode which is formed between the first and second gate insulation films. Therefore, the combination of the cited references still would not disclose or suggest these features, since none of the references teach or suggest this feature. Accordingly, withdrawal of the rejection is respectfully requested.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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